AMENDMENTS TO THE DRAWINGS

The attached sheet(s) of drawings includes changes to Figures as indicated in the Remarks.

Attachment: Replacement sheets

REMARKS

This communication is in response to the Office Action dated July 25, 2005. In that Office Action, the Examiner objected to the drawings as failing to comply with 37 CFR 1.84(p)(4). The Examiner also noted some typographical errors in the specification. Finally, the Examiner rejected the claims as being obvious in view of U.S. Patent No. 5,486,480 to Chen combined with U.S. Patent. No. 6,468,915 to Liu.

First, Figures 1A, 2A, 2D, 2E and 2G are amended according to the Examiner's suggestion for complying with 37 CFR 1.84(p)(4). The corrections include reference numeral 104 for FIG. 1A, numeral 202 in FIG. 2A, numeral 202a in FIG. 2D, numeral 205 in FIG. 2E, and numeral 308 in FIG. 2G. Additionally, FIGS. 1A-1C are designated as "Prior Art" as suggested by the Examiner. The specification and Claim 24 are also amended as suggested by the Examiner.

The Examiner argues that the Chen patent discloses a programmable transistor, that includes all of the elements of Claim 19 in the present invention. The Examiner also argues that Liu discloses a MOSFET with an isolation layer formed along the surface of the gate. Applicant respectfully disagrees with the Examiner. Chen discloses a programmable transistor including impurity regions to reduce punch-through and the soft-write phenomena. In order to provide fast operation, the impurity regions are arranged with regard to one another so that parasitic capacitances at junctions of impurity regions of mutually opposite conductivity type are minimized. Liu discloses a method for removing a silicon oxynitride ARC from over a polysilicon gate after the gate is patterned. The ARC is removed by wet etching without damaging or undercutting the polysilicon gate.

After the careful review of Chen and Liu, there is no indication or motivation to combine Chen and Liu to form a mask ROM of the present invention. The EPROM of Chen

is an erasable programmable read-only memory, but the information programmed in the mask ROM of the present invention is not erasable. EPROM and mask ROM are completely different in structure and operation mechanism, for example, the storage carrier of the EPROM is stored in a floating gate, but the mask ROM does not have a floating gate structure. Neither Liu or Chen is analogous art to the claimed invention.

Further, the mask ROM of the present invention may contain two bits of data: "digital zero" and "digital one," controlled by the different threshold voltage, which is not taught in the prior art. The claimed invention states that a "digital zero" area is defined in said source/drain formed at said unselected side, and "digital one" area is defined in said source/drain with extension source/drain. Both Chen and Liu fail to teach the digital one and digital zero areas of the claimed invention. The combination of Liu and Chen does not achieve the present claimed invention. Therefore, the non-obviousness rejection of the Claim 19 is overcome. Claims 20-25, which depend from Claim 19, are thus also patentable.

There is no motivation to form the mask ROM of the present invention by combining Chen, Liu, and Clevenger (U.S. Patent Application Publication No. 2002/0163039). Clevenger discloses a method and structure for a metal oxide semiconductor field effect transistor (MOSFET). As noted above, the combination of Chen and Liu fails to achieve the claimed invention. Therefore, the non-obviousness rejection of Claim 26 and 27 is also overcome.

In view of the forgoing, claims 19-30 pending in the application comply with the requirements of patentability define over the applied art. A notice of allowance is, therefore, respectively requested.

Applicant believes no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 50-0665, under Order No. 386998045US from which the undersigned is authorized to draw.

Dated:

10/24/05

Respectfully submitted,

By _____

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Attachments:
Replacement Sheet (3 pages)